

REMARKS

Responsive to the action mailed September 27, 2001, applicants elect the invention of Group II, Claims 18-37 and 39-40 drawn to the embodiment of a semiconductor device. The election is made without traverse.

Applicants further amend Claims 18-20, 23, 25, and 28-37 herein. Applicants add new Claims 41-56. Applicants submit all claims are in condition for allowance, and respectfully request the same.

Our check in the amount of \$468 for the excess claim fees was mailed on October 22, 2001. Please apply any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: _____

4/8/02



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Version with markings to show changes made

In the claims:

Claim 18-20, 23, 25, and 28-37 have been amended as follows:

18. (Amended) An integrated circuit [including]
comprising:

a CMOS circuit; [having]

an n-channel field effect transistor and a p-channel
field effect transistor[,]
in the CMOS circuit;

[at least] said n-channel field effect transistor
comprising:

a crystalline semiconductor formed on [an
insulative substrate or an insulating layer,]
an insulating surface;

[said crystalline semiconductor including] a
source region, a drain region and a channel forming region in
the crystalline semiconductor; [and]

a gate insulating film; [and]

a gate electrode formed [on] over the channel
forming region;[,]

said channel forming region comprising:

a plurality of carrier moving regions; [and]

a plurality of impurity regions,
wherein the plurality of impurity region of the
channel forming region are formed locally for pinning of a
depletion layer,

wherein the depletion layer [developing] is
formed from the drain region toward the channel forming region
and the source region,

wherein each of [said] the impurity regions
[containing] comprises an impurity element for shifting an
energy band in such a direction that movement of electrons is
obstructed.

19. (Amended) An integrated circuit [including]
comprising:

a memory circuit; [having]

a field effect transistor[,] in the memory circuit;

said field effect transistor comprising:

a crystalline semiconductor; [including]

a source region, a drain region and a channel
forming region in the crystalline semiconductor; [and]

a gate insulating film; [and]

a gate electrode formed [on] over the channel
forming region;[,]

said channel forming region comprising:

a plurality of carrier moving regions; [and]
a plurality of impurity regions,
wherein the plurality of the impurity region in
the channel forming region are formed locally for pinning of a
depletion layer,
wherein the depletion layer [developing] is
formed from the drain region toward the channel forming region
and the source region,
wherein each of [said] the impurity regions
[containing] comprises an impurity element for shifting an
energy band in such a direction that movement of electrons is
obstructed.

20. (Amended) An integrated circuit according to claim 18
[or 19],

wherein [said] the impurity element is for forming a
built-in potential difference locally in the channel forming
region.

23. (Amended) An integrated circuit according to claim 18
[or 19],

wherein [said] the impurity element belongs to group
XV.

25. (Amended) An integrated circuit according to claim 18 [or 19], wherein [said] the carrier moving regions are intrinsic or substantially intrinsic.

28. (Amended) An integrated circuit according to claim 18 [or 19],

wherein a width W of the channel forming region, a total width W_{pi} of the impurity regions, and a total width W_{pa} of regions between the impurity regions satisfy relationships $W_{pi}/W = 0.1$ to 0.9 , $W_{pa}/W = 0.1$ to 0.9 , and $W_{pi}/W_{pa} = 1/9$ to 9 .

29. (Amended) An integrated circuit according to claim 18 [or 19],

wherein in at least one cross-section taken by cutting the channel forming region in a direction perpendicular to a channel direction, the channel forming region is substantially regarded as a collection of a plurality of channel forming regions sectioned by the impurity regions.

30. (Amended) An integrated circuit according to claim 18 [or 19],

wherein a reduction in threshold voltage caused by a short channel effect occurring in the channel forming region during driving is compensated by an increase in threshold

voltage caused by a narrow channel effect obtained by utilizing the impurity regions.

31. (Amended) An integrated circuit according to claim 18 [or 19],

wherein the impurity regions serve as regions for buffering stress that occurs in the crystalline semiconductor.

32. (Amended) An integrated circuit according to claim 18 [or 19],

wherein a total width of the carrier moving regions is within a range of 30 to 3,000 Å.

33. (Amended) An integrated circuit according to claim 18 [or 19],

wherein [said] the impurity regions have dot patterns.

34. (Amended) An integrated circuit according to claim 18 [or 19],

wherein [said] the impurity regions have linear patterns substantially parallel with a channel direction.

35. (Amended) An integrated circuit according to claim 18 [or 19],

wherein a threshold voltage is controlled by
controlling widths of the carrier moving regions.

36. (Amended) An integrated circuit according to claim 18
[or 19],

wherein [said] the impurity element in [said] the
impurity regions is at a concentration of 1×10^{17} to 1×10^{20}
atoms/cm³.

37. (Amended) The integrated circuit of claim 18 [or 19]
in combination with at least an electric apparatus selected
from the group consisting of a liquid crystal display device, an
EL display device, a CL display device, a TV camera, a personal
computer, a car navigation apparatus, a TV projection apparatus,
a video camera, and a portable information terminal apparatus
including a cellular telephone and a mobile computer.

New Claims 41-56 have been added.